rated current. The Vp may possibly exceed the rated voltages of the diodes, for which some measures are required to be taken.

SUMMARY OF THE INVENTION

[0017] From the view of the above respects, it is an object of the present invention to provide a semiconductor device which can reduce a switch loss while avoiding increase of the conduction loss of an IGBT and securing a low noise characteristic, and also a power converter using the semiconductor device.

[0018] In accordance with an aspect of the present invention, the above object is attained by providing a semiconductor device which includes a semiconductor substrate having a pair of main surfaces; a first semiconductor region of a first conductivity type positioned adjacent to one of the main surfaces of the semiconductor substrate and located within the substrate; a second semiconductor region of a second conductivity type provided adjacent to the first semiconductor region and having a carrier concentration lower than the carrier concentration of the first semiconductor region; a third semiconductor region of the second conductivity type provided adjacent to the second semiconductor region and having a carrier concentration lower than the carrier concentration of the second semiconductor region; a plurality of MOS type trench gates extended from one of the main surfaces of the semiconductor substrate into the third semiconductor region to have at least two sorts of different intervals; a fourth semiconductor region of the first conductivity type provided between the MOS type trench gates having a narrow adjacent interval and having a carrier concentration higher than the carrier concentration of the third semiconductor region; a fifth semiconductor region of the second conductivity type provided between the MOS type trench gates having the narrow adjacent interval, located within the fourth semiconductor region to be adjacent to the MOS type trench gates, and having a carrier concentration higher than the carrier concentration of the fourth semiconductor region; a sixth semiconductor region of the first conductivity type located between the MOS type trench gates having the narrow adjacent intervals and having a carrier concentration higher than the carrier concentration of the third semiconductor region; a first electrode located between the MOS type trench gates having the narrow adjacent interval to be contacted with the fourth and fifth semiconductor regions; and a second electrode contacted with the first semiconductor region. The third semiconductor region is exposed to its main surface between the sixth semiconductor region and the trench gates.

[0019] In accordance with another aspect of the present invention, the above object is attained by providing a power converter which includes a pair of DC terminals, AC terminals corresponding in number to phases of an AC source, and a plurality of power conversion units connected between the pair of DC terminals. Each of the power conversion units has a series circuit of two parallel circuits each having a switching element and a diode of a polarity opposite to the switching element. The power conversion units have the AC terminals as different mutual interconnection points between the two parallel circuits. The switching element is the aforementioned semiconductor device.

[0020] In accordance with the present invention, the IGBT can avoid increase of a conduction loss, secure a low noise characteristic and also reduce a switch loss. The power converter for use in an inverter system or the like using the semiconductor device can increase an efficiency.

[0021] Other objects, features and advantages of the invention will become apparent from the following description of the embodiments of the invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. **1** shows a cross-sectional view of a semiconductor device in accordance with a first embodiment of the present invention;

[0023] FIG. **2** shows a cross-sectional view of a semiconductor device in accordance with a second embodiment of the present invention;

[0024] FIG. **3** shows a cross-sectional view of a semiconductor device in accordance with a third embodiment of the present invention;

[0025] FIG. **4** shows a cross-sectional view of a semiconductor device as a variation of the third embodiment;

[0026] FIG. **5** shows a cross-sectional view of a semiconductor device as another variation of the third embodiment;

[0027] FIG. **6** shows a cross-sectional view of a semiconductor device in accordance with a fourth embodiment of the present invention;

[0028] FIG. **7** shows a cross-sectional view of a semiconductor device in accordance with a fifth embodiment of the present invention;

[0029] FIG. **8** shows a cross-sectional view of a semiconductor device in accordance with a sixth embodiment of the present invention;

[0030] FIG. **9** shows a partial perspective view of a part of the sixth embodiment;

[0031] FIG. **10** is a partial perspective view of the embodiment showing another layout of gate termination ends and peripheral breakdown voltage structure in the present invention;

[0032] FIG. **11** shows a cross-sectional view of a semiconductor device in accordance with a seventh embodiment of the present invention;

[0033] FIG. **12** is a circuit configuration of a power converter in accordance with an eighth embodiment of the present invention;

[0034] FIG. **13** shows a cross-sectional view of a prior art semiconductor device;

[0035] FIG. **14** shows rated current turn-on waveforms of an IGBT and reverse recovery waveforms of diodes of a pair of arms in an inverter circuit;

[0036] FIG. **15** shows small current turn-on waveforms of the prior art IGBT and reverse recovery waveforms of diodes of a pair of arms in an inverter circuit;

[0037] FIG. **16** shows small current turn-on waveforms of an IGBT to which the present invention is applied and reverse recovery waveforms of diodes of a pair of diodes in an inverter circuit;

[0038] FIG. **17** is a graph for explaining a difference in structure between the prior art and the present invention; and

[0039] FIG. **18** is a graph for explaining another difference in structure between the prior art and the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0040] Embodiments of the present invention will be explained with reference to the attached drawings.

Embodiment 1

[0041] FIG. **1** shows a cross-sectional view of a semiconductor device in accordance with a first embodiment of the